IDS #7

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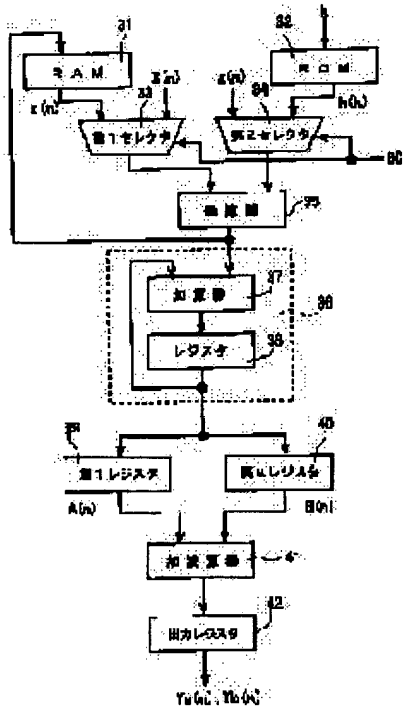
(54) DIGITAL FILTER

(57)Abstract:

PROBLEM TO BE SOLVED: To incorporate an attenuating function in the digital filter.

SOLUTION: Input data X(n) is inputted to a multiplier 35 through a selector 33 and multiplied by an attenuation coefficient g(m) inputted through a selector 34 and the result is stored as attenuation input data x(n) in a RAM 31. The attenuation input data x(n) read out of the RAM 31 is inputted to a multiplier 35 through the selector 34 and supplied to a cumulating adder 36. The multiplication data is cumulatively added by the cumulating adder 36 according to the number of taps and final cumulative addition data are stored as intermediate data A(n) and B(n) in registers 39 and 40 alternately. An adder subtracter 41 performs a subtracting process and an adding process for the intermediate data A(n) and B(n) and output data Ya(n) and Yb(n) are stored in an output register 42.



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* NOTICES *

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] This invention relates to the digital filter which separates the digital data used for a digital audio device etc.
[0002]
[Description of the Prior Art] As shown in a formula (1), the digital filter of an FIR mold (Finite Impulse Responce) is constituted so that output-data Y (n) may be obtained by the convolution of input data X (n) and an impulse response.
[0003]
[Equation 1]

$$Y(n)=\sum_{k=0}^{N-1} h(k)\cdot X(n-k) \qquad \cdots (1)$$

[0004] Here, h (k) is a filter factor and N is the number of taps. Then, it is [0005] when the Z transform of the formula (1) is carried out.
[Equation 2]

$$H(z)=\sum_{n=0}^{N-1} h(n)\cdot Z^{-n} \qquad \cdots (2)$$

[0006] It is [0007] from ******** and this formula (2).
[Equation 3]

$$H(e^{j\omega})=\sum_{n=0}^{N-1} h(n)\cdot e^{-j\omega n} \qquad \cdots (3)$$

[0008] A next door and a frequency response are known. And a formula (3) is [0009] when omega=2pik/N.
[Equation 4]

$$H(e^{j\omega})=\sum_{n=0}^{N-1} h(n)\cdot e^{-j2\pi nk/N} \qquad \cdots (4)$$

[0010] It becomes. It can be considered that this formula (4) is the formula of a discrete Fourier transform (DFT:Discrete Fourier Transform). Therefore, filter factor h (k) is called for by carrying out inverse transformation (IDFT:Inverse Discrete Fourier Transform) of the frequency characteristic given by the formula (4). Drawing 5 is the circuit diagram showing the configuration of the digital filter of a standard FIR mold.
[0011] Two or more delay elements 1 are constituted by the shift register, it connects with a serial mutually, and only a respectively fixed period T is delayed in input data X (n). It connects with the input side of input data X (n), and the output side of each delay element 1, respectively, and two or more multipliers 2 carry out the multiplication of the filter factor [of a proper] h (k) to input data X (n) and

the output of each delay element 1, respectively. Thereby, convolution processing of an impulse response is performed to input data X (n).

[0012] The output of each multiplier 2, i.e., predetermined filter factor h, (k) takes total of input data X (n) by which multiplication was carried out, and the output of each delay element 1, and it outputs the total adder 3 as output-data Y (n). Therefore, it means that the operation according to an above-mentioned formula (1) was performed to input data X (n). Since a delay element 1 and a multiplier 2 are arranged according to the number N of taps, such a digital filter has the problem that a circuit scale becomes large with the increment which is the number N of taps. Then, the input data of time series is once memorized in memory, and the digital filter of the stored program which was made to ****** the multiplication result is proposed, carrying out the multiplication of the filter factor to the input data read from the memory one by one.

[0013] Drawing 6 is the block diagram showing the configuration of the digital filter of a stored program. RAM11 carries out the sequential storage of the input data X (n) inputted by time series, and ROM12 memorizes two or more filter factor h (k) beforehand. Moreover, RAM11 reads and outputs memorized input data X (n) for every step, and ROM12 reads and outputs specific filter factor h (k) corresponding to the value of k which increases for every step. In addition, this k is a match at k shown in the formula (1). And a multiplier 13 carries out the multiplication of the filter factor h (k) by which reading appearance was carried out to input data X (n-k) by which reading appearance was carried out from RAM11 from ROM12.

[0014] Acceleration **** 14 consists of an adder 15 and a register 16, and ****** the multiplication result of a multiplier 13. That is, the output of a multiplier 13 and the output of a register 16 are added by the adder 15, and sequential addition of the multiplication result of a multiplier 13 is carried out by storing the addition result in a register 16 again. An output register 17 incorporates acceleration ****** outputted from acceleration **** 14, and outputs it as output-data Y (n).

[0015] in this FIR mold digital filter, by carrying out reading appearance of the input data X (n) and filter factor h (k) one by one from RAM11 and ROM12, respectively, and repeating a sum-of-products operation, the operation according to a formula (1) was performed and output-data Y (n) has been obtained. For this reason, a circuit scale does not become large even if the number N of taps becomes large. By the way, it is [0016] to the digital filter which has the 1st filter factor h1 (n).

[Equation 5]

$$h_2(n) = (-1)^n \cdot h_1(n) \qquad \cdots (5)$$

[0017] The digital filter which has the 2nd filter factor h2 (n) which is alike and is given more is called a mirror filter from the frequency response nature. The relation of the Z transform in such a mirror filter is [0018].

[Equation 6]

$$\begin{aligned} H_2(z) &= \sum_{n=-\infty}^{\infty} Z^{-n} \cdot h_2(n) \\ &= \sum_{n=-\infty}^{\infty} Z^{-n} \cdot (-1)^{-n} \cdot h_1(n) \qquad (6) \\ &= H_1(-Z) \end{aligned}$$

[0019] It comes out. Here, considering frequency response nature, it is [0020].

[Equation 7]

$$h_2(n) = e^{j\pi n} \cdot h_1(n) \qquad \cdots (7)$$

[0021] It comes out and a certain thing to a formula (6) is [0022].

[Equation 8]

$$H_2(e^{j\omega}) = H_1(e^{j\omega + j\pi}) \qquad \cdots (8)$$

[0023] It becomes. It turns out that the frequency response nature of a mirror filter becomes symmetrical

by this at pi/2. Here, since pi/2 is 1/4 of a sampling period, this mirror filter is called QMF (Quadrature Mirror Filter). Such QMF is explained by 522nd (IEEE Trans.Acoust., Speech, Signal Process., Vol.ASSP-32, No.3, June1984) page - the 531st page in full detail in IEEE transactions-on AKOSU tex speech - and - signal processing, ray S ESUPI 32 volume 3 No., and June, 1984.
[0024] As the separation filter with which band separation of a frequency component is performed is shown in a formula (9) and a formula (10), it is constituted by above-mentioned QMF by convolution processing with input data X (n) and an impulse response, and those addition or subtraction processing so that two output data Ya (n) and Yb (n) which are separation data of input data X (n) may be obtained.

[0025]
[Equation 9]

$$Ya(n)=\sum_{k=N-1}^{0} h(2k)\cdot X(2n-2k)-\sum_{k=N-1}^{0} h(2k+1)\cdot X(2n-2k+1) \quad \cdots (9)$$

[0026]
[Equation 10]

$$Yb(n)=\sum_{k=N-1}^{0} h(2k)\cdot X(2n-2k)+\sum_{k=N-1}^{0} h(2k+1)\cdot X(2n-2k+1) \quad \cdots (10)$$

[0027] Drawing 7 is the block diagram showing the configuration of the separation filter with which band separation processing in which a formula (9) and a formula (10) are followed is performed. Two or more delay elements 21 are connected to a serial, and only a fixed period T is delayed in input data X (n), respectively. It connects with the input side of input data X (n), and the output side of the delay element 21 of even level, and two or more 1st multipliers 22 carry out the multiplication of the filter factor h (2k) to input data X (n) and the output of each delay element 21, respectively. Moreover, it connects with the output side of the delay element 21 of odd level, and two or more 2nd multipliers 24 carry out the multiplication of the filter factor h (2k+1) to the output of each delay element 21, respectively. Thereby, convolution processing of an impulse response to input data X (n) is performed.
[0028] The 1st total adder 24 adds the whole of each output of the 1st multiplier 22, and outputs the middle data An. On the other hand, the 2nd total adder 25 adds the whole of each output of the 2nd multiplier 23, and outputs the middle data Bn. A subtractor 26 subtracts the middle data Bn inputted from the 2nd total adder 25 from the middle data An inputted from the 1st total adder 24, and outputs it as the 1st output data Ya (n). Moreover, an adder 27 adds the middle data An inputted from the 1st total adder 24, and the middle data Bn inputted from the 2nd total adder 25, and outputs it as 2nd output-data Yb (n). Thus, data processing according to a formula (9) and a formula (10) is attained.
[0029] Constituting the above separation filters with an above-mentioned stored program is indicated by JP,7-131295,A proposed by these people.
[0030]
[Problem(s) to be Solved by the Invention] In common audio equipment, the attenuation function which is made to decrease a sound signal and lowers playback sound volume is prepared. In the case of the digital audio device represented by MD (Mini Disc) player, by carrying out the multiplication of the attenuation coefficient from which gain becomes digitized audio data or less with one, it is constituted so that an attenuation function may be realized.
[0031] In data processing of digital data, when the number of multipliers with a large circuit scale increases, a processing unit becomes complicated and will cause an increase in cost. In the case of audio data with much number of bits, the increment in a multiplier tends [especially] to influence an increase in cost greatly. Then, this invention aims at making an attenuation function build in a digital filter, without increasing a circuit scale.
[0032]
[Means for Solving the Problem] A place by which accomplished in order that this invention might solve an above-mentioned technical problem, and it is characterized [the] Attenuation input data

generated based on time series input data and this time series input data It is inputted with a predetermined attenuation coefficient and a filter factor corresponding to the above-mentioned attenuation input data. A selector which chooses one group of the groups of a group of the above-mentioned time series input data and the above-mentioned predetermined attenuation coefficient or the above-mentioned attenuation input data, and the above-mentioned filter factor, A multiplier which carries out the multiplication of the group of select data of the above-mentioned selector mutually, and RAM which memorizes the result of an operation of the above-mentioned time series input data and the above-mentioned multiplier to a group of a predetermined attenuation coefficient, and is supplied to the above-mentioned selector as the above-mentioned attenuation input data, Acceleration **** which ****** the result of an operation of the above-mentioned attenuation input data and the above-mentioned multiplier corresponding to a group of the above-mentioned filter factor one by one, The 1st and 2nd registers which incorporate the result of an operation of the above-mentioned acceleration **** by turns, It has an adder subtracter which adds or subtracts the two results of an operation taken out from the 1st and 2nd registers of the above, and is in outputting the result of an operation of the above-mentioned adder subtracter as 1st [used as separation data of the above-mentioned input time series data], and 2nd output time series data.

[0033] According to this invention, the multiplication of the predetermined attenuation coefficient is carried out to input time series data, and RAM memorizes. And the multiplication of the filter factor is carried out to input time series data by which attenuation processing was carried out, and data processing for band separation is performed. It is not necessary to increase the number of multipliers by using a common multiplier by multiplication of an attenuation coefficient, and multiplication of a filter factor.

[0034]

[Embodiment of the Invention] Drawing 1 is the block diagram showing the 1st operation gestalt of the digital filter of this invention. It connects with the multiplier 35 mentioned later, and predetermined carries out period storage, it is being begun to read the attenuation input data x (n) inputted from a multiplier 35 for every step of the data processing one by one, and RAM31 outputs it. ROM32 memorizes two or more filter factor h (k) beforehand, corresponding to the value of k which increases for every step, reads predetermined filter factor h (k), and carries out a repeat output. This k is a match at k shown in the above-mentioned formula (9) - the formula (10). It connects with an encoding input and RAM31, and the 1st selector 33 chooses and outputs either of the attenuation input data x (n) by which reading appearance is carried out from input data X (n) or RAM31 of time series. It connects with an attenuation input and ROM32, and the 2nd selector 34 chooses and outputs either of the filter factor h (k) by which reading appearance is carried out from attenuation coefficient g (m) or ROM32. The selection control of these 1st and 2nd selectors 33 and 34 is answered and carried out to the common selection-control signal SC.

[0035] It connects with the 1st selector 33 and 2nd selector 34, and a multiplier 35 carries out the multiplication of either [either input data X (n) chosen by the 1st selector 33 or the attenuation input data x (n) and / which were chosen by the 2nd selector 34] attenuation coefficient g (m) or filter factor h (k). Here, when the 2nd selector 34 chooses attenuation coefficient g (m) when the 1st selector 33 chooses input data X (n), and the 1st selector 33 chooses the attenuation input data x (n), it operates by carrying out so that the 2nd selector 34 may choose filter factor h (k). Thereby, a multiplier 35 performs multiplication with input data X (n) and attenuation coefficient g (m), or the multiplication of the attenuation input data x (n) and filter factor h (k). And multiplication data with input data X (n) and attenuation coefficient g (m) is supplied to RAM31, and the attenuation input data x (n) and multiplication data with filter factor h (k) are supplied to acceleration **** 36.

[0036] It connects with a multiplier 35 and acceleration **** 36 which consists of an adder 37 and a register 38 ****** the multiplication data inputted from a multiplier 35 according to the number of taps. That is, the multiplication data of a multiplier 35 is ******(ed) by adding the multiplication data inputted from the data read from the register 38, and a multiplier 35 with an adder 37, and storing the addition data in a register 38 again.

[0037] It connects with acceleration **** 36, and the ****** data continuously inputted from acceleration **** 36 is incorporated by turns, and the 1st register 39 and 2nd register 40 store it, and output it to predetermined timing, respectively. For example, it is constituted so that middle data A (n) outputted from acceleration **** 36 to the oddth may be stored in the 1st register 39 and middle data B (n) outputted to the eventh may be stored in the 2nd register 40. It connects with the 1st register 39 and 2nd register 40, and an adder subtracter 41 subtracts or adds middle data A (n) by which reading appearance is carried out from each registers 39 and 40, and B (n).
[0038] It connects with an adder subtracter 41, and an output register 42 stores the addition-and-subtraction data inputted from an adder subtracter 41 for every data processing, and outputs it as output data Ya (n) and Yb (n). For example, it corresponds to the adder subtracter 41 which repeats a subtraction operation and an add operation by turns, subtraction data is outputted as output data Ya (n), and addition data is outputted as output-data Yb (n). The output of this output register 42 turns into an encoding output.
[0039] A multiplier 35 performs the multiplication of attenuation coefficient g (m), and the multiplication of filter factor h (k) by time sharing, and the above digital filter generates the output data Ya (n) and Yb (n) to which attenuation processing and separation processing were performed to input data X (n). Thereby, it becomes possible to perform attenuation processing, without adding a new multiplier in a digital filter.
[0040] Drawing 2 is a timing chart where the digital filter shown in drawing 1 explains the actuation at the time of setting the number N of taps to "4", and shows the time of n= 4. First, the 1st selector 33 chose input data X (n), and the 2nd selector 34 has chosen attenuation coefficient g (m). In this condition, if input data X (8) is inputted, in a multiplier 35, multiplication with input data X (8) and attenuation coefficient g (1) will be performed, and its multiplication data x(8) (=X(8) and g (1)) will be written in RAM31 as attenuation input data. Here, about attenuation coefficient g (1), the degree of the attenuation to input data X (n) is determined, and it is usually fixed to constant value. And when the writing to RAM31 of the attenuation input data x (8) is completed, the 1st selector 33 is switched to the attenuation input data x (8) side (RAM31 side), and the 2nd selector 34 is switched to coincidence at the filter factor h (k) side (ROM32 side).
[0041] Separation processing of the data based on a digital filter is performed to the attenuation input data x (8) memorized by RAM31. That is, input data X (n) is transposed to the attenuation input data x (n), and data processing according to the following formulas (11) and formulas (12) which calculate a formula (9) and a formula (10) as N= 4 taps, and are obtained is performed.
[0042]
[Equation 11]

$$Ya(n)=h(6)\cdot x(2n-6)+h(4)\cdot x(2n-4)+h(2)\cdot x(2n-2)+h(0)\cdot x(2n)$$
$$-h(7)\cdot x(2n-7)-h(5)\cdot x(2n-5)-h(3)\cdot x(2n-3)-h(1)\cdot x(2n-1) \quad \cdots (11)$$

[0043]
[Equation 12]

$$Yb(n)=h(6)\cdot x(2n-6)+h(4)\cdot x(2n-4)+h(2)\cdot x(2n-2)+h(0)\cdot x(2n)$$
$$+h(7)\cdot x(2n-7)+h(5)\cdot x(2n-5)+h(3)\cdot x(2n-3)+h(1)\cdot x(2n-1) \quad \cdots (12)$$

[0044] In drawing 2 , although illustration is omitted about the writing of input data X (0) - X (7), input data X (0) - X (7) are inputted ahead of input data X (8), and the multiplication of the attenuation coefficient g (1) is carried out, and they are memorized by RAM41 as attenuation input data x(0) -x(7), respectively. About the 1st and 2nd selectors 33 and 34, it is switched corresponding to multiplication processing with input data X (0) - X (7), and attenuation input data x(0) -x(7).
[0045] First, if reading appearance of the attenuation input data x (8) is carried out through the 1st

selector 33 from RAM31 and reading appearance of the filter factor h (0) is carried out through the 2nd selector 34 corresponding to this from ROM32, the multiplication of these will be carried out by the multiplier 35, and the multiplication data will be supplied to acceleration **** 36. At this time, the data of acceleration **** 36 is cleared and is stored in a register 38 as it is as data with which the multiplication value of the attenuation input data x (8) and filter factor h (0) =h (0) and x A(1) x (8) Becomes. Then, while reading appearance of the attenuation input data x (6), x (4), and x (2) is carried out to order from RAM31, reading appearance of filter factor h (2), h (4), and the h (6) is carried out to order from ROM32, multiplication is carried out by the multiplier 35, respectively, and each multiplication data is supplied to sequential acceleration **** 36. In acceleration **** 35, the multiplication data inputted is ******(ed) and sequential storing of the data which becomes A(2) =h (2) and x (6) A[+A1] (3) =h (4) and x (4) A[+A2] (4) =h (6) and x (2)+A3 is carried out at a register 38. And the data which was finally stored and +h (6) and x A(4) x [=h (0) and] (8) x [+h (2) and] (6) x [+h (4) and] (4) x (2) Becoming is stored in the 1st register 39.

[0046] Then, if reading appearance of the attenuation input data x (7) is carried out through the 1st selector 33 from RAM31 and reading appearance of the filter factor h (1) is carried out through the 2nd selector 34 corresponding to this from ROM32, the multiplication of these will be carried out by the multiplier 35, and the multiplication data will be supplied to acceleration **** 36. At this time, the register 38 of acceleration **** 36 is cleared and is stored in a register 38 as it is as data with which the multiplication value of the attenuation input data x (7) and filter factor h (1) =h (1) and x B(1) x (7) Becomes. Then, while reading appearance of the attenuation input data x (5), x (3), and x (1) is carried out to order from RAM31, reading appearance of filter factor h (3), h (5), and the h (7) is carried out to order from ROM32, and sequential supply of each multiplication data is carried out at acceleration **** 36. Therefore, sequential storing of the data which becomes B(2) =h (3) and x (5) B[+B1] (3) =h (5) and x (3) B[+B-2] (4) =h (7) and x (1)+B3 is carried out at a register 38. And the data which was finally stored and +h (7) and x B(4) x [=h (1) and] (7) x [+h (3) and] (5) x [+h (5) and] (3) x (1) Becoming is stored in the 2nd register 40.

[0047] And data A (4) and B (4) are inputted into an adder subtracter 41 from the 1st register 39 and 2nd register 40, respectively, data A (4) and data B (4) is added, and data B (4) is further subtracted from data A (4).